when said integrated circuit element is in normal operation, said test pad is electrically disconnected from the outside of said semiconductor integrated circuit device.

REMARKS

The Applicants request reconsideration of the rejection.

A new title has been provided as required by the Examiner.

Claims 1-3, 9, 15-18, 23-24 and 26-27 were rejected under 35 USC §102(e) as being anticipated by Yoshida, US 6,445,001. Claims 4-8, 19-22, 25 and 28 were rejected under 35 USC §103(a) as being unpatentable over Yoshida in view of Iwabuchi, US 6,030,890. The Applicants traverse as follows.

It is noted that claims 15-22 have been canceled without prejudice, the Applicants retaining their right to resubmit these claims in a continuation application. Claims 10-14 have also been canceled as being directed to a non-elected invention. Accordingly, claims 1-9 and 23-28 are pending and rejected.

The pending claims patentably define over Yoshida and Iwabuchi, whether taken individually or in combination. In each of the independent claims 1-2 and 23-28, the invention requires that the semiconductor integrated circuit device have

a protruding (bump) electrode and a testing pad that is not coupled to the protruding electrode. Further, the protruding electrode and the testing pad must be exposed from an insulating film covering the electrode surface of the device.

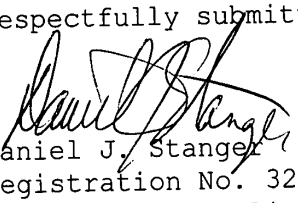
According to this feature, testing pads can be provided independently of the bump electrodes, which can thus be reserved for signal input/output or power. It is not necessary to provide bump electrodes for connection to the testing pads. Therefore, the device manufacturer can perform burn-in testing after dicing, and after formation of the bump electrodes. Custom-engineered burn-in sockets are not necessary, so that conventional "universal" burn-in sockets can be used. Furthermore, the burn-in processing for each chip unit can be easily performed, contributing to a reduction in the testing cost.

The Applicants refer the Examiner to Figs. 36 and 44, and page 88, line 15 through page 92, line 18 for a discussion.

Neither Yoshida nor Iwabuchi teaches or fairly suggests the provision of testing pads that are distinct from the protruding or bump electrodes, and exposed from an insulating film covering the surface. Accordingly, the combination of these documents does not reach the claimed invention.

In view of the foregoing amendments and remarks, the Applicants request reconsideration of the rejection and allowance of the claims.

Respectfully submitted,



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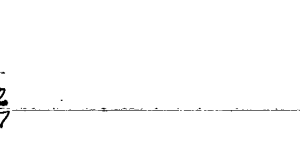
on 3/24/03 by 

MARKED-UP VERSION OF REPLACED PARAGRAPH(S) OF THE SPECIFICATION

Page 10, first full paragraph (lines 4-19), the marked-up paragraph is as follows:

An electric fuse is known as another program element. For example, USP No. [5,110,753] 5,110,754 has described a technology wherein an antifuse corresponding to a kind of electric fuse is used for defective relief or the like of a DRAM. The antifuse has a configuration capable of being programmed by dielectric breakdown of an oxide film held in an insulating state. Further, USP No. 5,742,555 has shown, as an example of an antifuse, an example in which an oxide film is used to form a capacitor in a p-type well region, and a negative voltage is applied to a well electrode of the capacitor and a positive voltage is applied to a plate electrode on the oxide film to thereby bring a gate oxide film into dielectric breakdown. As other references each having described a semiconductor integrated circuit using an electric fuse, there are known USP No. 5,324,681, etc.

MARKED-UP VERSION OF REWRITTEN CLAIM(S)

1. (Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a plurality of circuit elements formed in an element forming layer on said semiconductor substrate;

a plurality of first and second terminals formed on the surface of said element forming layer and connected to predetermined ones of said circuit elements;

a plurality of conductive layers which are respectively connected to said first terminals corresponding to some terminals of said plurality of terminals and [extend] extending on said element forming layer;

protruding electrodes respectively connected to said conductive layers;

testing pads respectively connected to [all or some of second terminals corresponding to the remaining terminals of said plurality of terminals] said second terminals, said testing pads being not coupled to any protruding electrode; and

an insulating film which covers the surfaces of said protruding electrodes and said testing pads so as to expose said protruding electrodes and said testing pads.

2. (Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a plurality of circuit elements formed in an element forming layer on said semiconductor substrate;

[a plurality of] first and second terminals formed on the surface of said element forming layer and connected to predetermined ones of said circuit elements;

a [plurality of] conductive [layers] layer which [are respectively] is connected to said first terminal [terminals corresponding to some of said plurality of terminals and extend on said element forming layer];

a protruding [electrodes respectively] electrode connected to said conductive [layers] layer;

a testing [pads respectively] pad connected to [all or some of] said second [terminals corresponding to the remaining terminals of said plurality of terminals and all or some of the first terminals] terminal, said testing pad being not coupled to any protruding electrode; and

an insulating film which covers the surfaces of said protruding [electrodes] electrode and said testing [pads] pad so as to expose said protruding [electrodes] electrode and said testing [pads] pad.

5. (Amended) The semiconductor integrated circuit device according to claim 3, wherein said insulating film is a film which contains an organic substance.

9. (Amended) The semiconductor integrated circuit device according to claim [1] 3, wherein said testing pads extend on said further insulating film.

23. (Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a first circuit element and a second circuit element formed on said semiconductor substrate;

a wiring [wirings] formed over said semiconductor substrate and [each] connected to said first circuit element;

a bump [bumps] formed over said [wirings] wiring and connected thereto; and

a conductive layer, which is formed over said semiconductor substrate and connected to said second circuit element and which constitutes a testing [pads] pad,

wherein said conductive layer is electrically isolated from any bump.

24. (Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a semiconductor integrated circuit element formed in said semiconductor substrate;

a wiring formed on said semiconductor substrate and connected to said semiconductor integrated circuit element;

a bump formed on said wiring and connected thereto; and

a conductive layer, which is formed on said semiconductor substrate and connected to said semiconductor integrated circuit element and which constitutes [each of] a testing [pads] pad which is electrically isolated from any bump,

wherein when said semiconductor integrated circuit element is tested, said testing pad is electrically connected to the outside of said semiconductor integrated circuit device, and

when said semiconductor integrated circuit element is in normal operation, said testing pad is electrically disconnected from the outside of said semiconductor integrated circuit device.

25. (Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

integrated circuit elements formed on said semiconductor substrate;

a plurality of wirings formed on said semiconductor substrate and connected to said integrated circuit elements;

a plurality of bumps, formed on said plurality of wirings and provided in association with said plurality of wirings;

a conductive layer, which is formed on said semiconductor substrate and connected to said integrated circuit elements and which is formed as [each of] a testing [pads] pad which is electrically isolated from any bump; and

an organic film placed on said semiconductor substrate and formed below said plurality of wirings,

wherein when said each integrated circuit element is tested, each said [each] testing pad is electrically connected

to the outside of said semiconductor integrated circuit device, and

when each said [each] integrated circuit element is in normal operation, each said [each] testing pad is electrically disconnected from the outside of said semiconductor integrated circuit device.

26. (Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a first circuit element and a second circuit element formed on said semiconductor substrate;

a wiring formed on said semiconductor substrate and connected to said first circuit element;

a bump formed on said wiring and connected thereto;

a first conductive material, which is formed on said semiconductor substrate and connected to said first circuit element and which constitutes a first testing pad; and

a second conductive material, which is formed on said semiconductor substrate and connected to said second circuit element and which constitutes a second testing pad which is not connected to any bump,

wherein when said first circuit element and said second circuit element are tested, said first testing pad and said second testing pad are electrically connected to the outside of said semiconductor integrated circuit device, and

when said first circuit element and said second circuit element are in normal operation, said first testing pad is electrically connected to the outside of said semiconductor integrated circuit device through said bump, and said second testing pad is electrically disconnected from the outside of said semiconductor integrated circuit device.

27. (Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

an integrated circuit formed on said semiconductor substrate;

a wiring formed on said semiconductor substrate and connected to said integrated circuit;

a bump formed on said wiring and connected thereto;

a first conductive layer, which is formed on said semiconductor substrate and connected to said integrated circuit and which constitutes a first testing pad; and

a second conductive layer, which is formed on said semiconductor substrate and connected to said integrated circuit and which constitutes a second testing pad which is not connected to any bump,

wherein said first conductive layer and said wiring are connected to each other, and

when said integrated circuit is tested, said first testing pad and said second testing pad are electrically connected to the outside of said semiconductor integrated circuit device and

when said integrated circuit is in normal operation, said first testing pad is electrically connected to the outside of said semiconductor integrated circuit device and said second testing pad is electrically isolated from the outside of said semiconductor integrated circuit device.

28. (Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

integrated circuit elements formed on said semiconductor substrate;

a plurality of wirings formed over said semiconductor substrate and connected to at least one of said integrated circuit elements;

a plurality of bumps formed over said plurality of wirings and provided in association with said plurality of wirings;

a conductive layer, which is formed over said semiconductor substrate and connected to at least one of said [each] integrated circuit [element] elements and which constitutes [each of] a test [pads] pad which is not connected to any bump; and

a film containing an organic material formed between said semiconductor substrate and said plurality of wirings and between said semiconductor substrate and said conductive layer,

wherein when said integrated circuit element is tested, said test pad is electrically connected to the outside of said semiconductor integrated circuit device, and

when said integrated circuit element is in normal operation, said test pad is electrically disconnected from the outside of said semiconductor integrated circuit device.